FAST LOCALIZATION OF ELECTRICAL FAILURES ON AN INTEGRATED CIRCUIT SYSTEM AND METHOD

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 60/432,786, filed December 11, 2002, the entire content of which is incorporated herein by reference.

BACKGROUND

1. Field of the Invention

[0002] The present application relates to fast localization of electrical failures on an integrated circuit.

2. Related Art

[0003] The fabrication of integrated circuits is an extremely complex process that may involve hundreds of individual operations. For a number of reasons, defects can be introduced into the integrated circuits during these operations. For example, in photoresist and photomask operations, the presence of contaminants such as dust, minute scratches and other imperfections in the patterns on the photomasks can produce defective patterns on the semiconductor wafers, resulting in defective integrated circuits.

[0004] Defective integrated circuits may be identified both by visual inspection under high magnification and by electrical tests. Once a defective integrated circuit has been identified, the location of the defect in the integrated circuit is typically determined to permit closer inspection of the defect. Conventional techniques for detecting and localizing the defects typically test integrated circuits individually, which can be time consuming, particularly when the number of integrated circuits being tested is large.

SUMMARY

[0005] In one exemplary embodiment, fast localization of electrically measured defects of integrated circuits includes providing information for fabricating a test chip having test structures configured for parallel electrical testing. The test structures on the test chip are

electrically tested employing a parallel electrical tester. The results of the electrical testing are analyzed to localize defects on the test chip.

DESCRIPTION OF DRAWING FIGURES

[0006] The present application can be best understood by reference to the following description taken in conjunction with the accompanying drawing figures, in which like parts may be referred to by like numerals:

[0007] Fig. 1 is a flow diagram of an exemplary process of localizing defects on a test chip;

[0008] Fig. 2 is a flow diagram of another exemplary process of localizing defects on a test chip;

[0009] Fig. 3 is a flow diagram of another exemplary process of localizing defects on a test chip;

[0010] Fig. 4 is a block diagram of an exemplary system to localize defects on a test chip;

[0011] Fig. 5 depicts a product chip with design pattern variations;

[0012] Fig. 6 depicts an exemplary layout of a test chip;

[0013] Fig. 7 depicts an exemplary padgroup;

[0014] Figs. 8 and 9 depict exemplary test structures;

[0015] Fig. 10 depicts another exemplary padgroup;

[0016] Figs. 11, 12-A, 12-B, and 12-C depict exemplary test structures;

[0017] Fig. 13 depicts another exemplary padgroup.

[0018] Figs. 14-21 depict portions of another exemplary layout;

[0019] Fig. 22 depicts another exemplary layout;

[0020] Fig. 23 is a front view of an exemplary parallel tester;

[0021] Fig. 24 is a side of the exemplary parallel tester depicted in Fig. 23;

[0022] Fig. 25 is a top view of an exemplary wafer tester system;

[0023] Fig. 26 is a perspective view of the exemplary wafer tester system depicted in Fig. 25;

[0024] Fig. 27 is a system block diagram of the wafer tester system depicted in Fig. 25;

[0025] Fig. 28 is a system block diagram of a portion of the wafer tester system depicted in Fig. 25;

[0026] Fig. 29 is a circuit diagram of a resistor divider;

[0027] Fig. 30 is a circuit diagram of a two point resistance measurement implementation;

[0028] Fig. 31 is a system block diagram of a portion of a switch card;

[0029] Fig. 32 is a circuit diagram of a portion of a pin terminator circuit;

[0030] Fig. 33 is a system block diagram of a measurement control (MC) unit;

[0031] Fig. 34 depicts an exemplary process of defect analysis; and

[0032] Figs. 35, 36, and 37 depict exemplary plots of failure rate vs. layout bins;

DETAILED DESCRIPTION

[0033] The following description sets forth numerous specific configurations, parameters, and the like. It should be recognized, however, that such description is not intended as a limitation on the scope of the present invention, but is instead provided as a description of exemplary embodiments.

[0034] I. Overview

[0035] With reference to Fig. 1, in one exemplary embodiment, a process of localizing defects on a test chip is depicted. As will be described below in greater detail, a test chip includes a plurality of test structures, which are designed to simulate failure modes that may result in fabricating an integrated circuit of an actual product chip.

[0036] In block 102, a test chip is fabricated on a test wafer. The test chip includes a plurality of test structures and probe pads. A test structure is electrically connected to one or more probe pads, which are used to electrically test the test structure.

[0037] In one exemplary embodiment, the test structures of the test chip are configured for parallel electrical testing. More specifically, test structures are grouped together as one or more padgroups. The test structures in a padgroup are electrically tested in parallel, meaning that the test structures are electrically tested together at approximately the same time.

[0038] In another exemplary embodiment, the test structures of the test chip are configured for localization of defects. More specifically, if a test structure on a test chip is fabricated with a defect that results in the test structure failing the electrical test performed on the test structure, the location of the test structure with the defect within the test chip is obtained.

[0039] In block 104, the test structures on the test chip are electrically tested in parallel. In one exemplary embodiment, the test structures in a padgroup are electrically tested in parallel, meaning that they are electrically tested together at approximately the same time. Additionally, multiple padgroups can be electrically tested in parallel. Thus, in this manner, the amount of time required to electrically test the test structures on the test chip may be reduced.

[0040] In block 106, the results of the electrical test performed on the fabricated test chips are analyzed. More specifically, a test structure that fails the electrical test is assumed to have been fabricated with a defect. Thus, the electrical test detects defects on the test chip. In one exemplary embodiment, the detected defects are classified as random or systematic defects. Additionally, in one exemplary embodiment, when a test structure with a defect is identified, the location of the test structure within the test chip is obtained.

[0041] It should be noted that the exemplary process described above and depicted in Fig. 1 can include various additional steps. For example, with reference to Fig. 2, in one alternative embodiment, in block 202, the fabricated chip can be in-line inspected. More specifically, the fabricated chip can be in-line inspected using an optical inspection tool, such as a microscope, to visually detect any defects on the fabricated test chip and to determine the location of the defects. As depicted in Fig. 2, the results of the analysis performed in block 106 can be used as a feedback to the in-line inspection performed in block 202.

[0042] With reference to Fig. 3, in another alternative embodiment, in block 302, the results of the analysis performed in block 106 can be used to inspect the defects using an inspection tool, such as an optical inspection tool, a defect review scanning electron microscope (DR-SEM), a wafer inspection scanning electron microscope (SEM), and the like. More specifically, the results of the electrical test can localize (i.e., identify the location of) the test structure with a defect within the test chip. The inspection tool can then inspect the test structure to localize the defect to a specific location within the test structure. The inspection tool can also obtain an image of the defect, which can then be used to further analyze the defect, such as measuring the size of the defect, classifying the defect, and identifying a potential cause of the defect. It should be recognized that block 202 can be omitted from the present exemplary embodiment.

[0043] In this alternative embodiment, the test chip is adapted for use with the inspection tool. More specifically, the test structures on the test chip are sized to be compatible with the capabilities of an inspection tool, such as the view field of the inspection tool, which determines the area that can be inspected at one time, and the resolution of the inspection tool, which determines the amount of detail that can be obtained. For example, when a test structure is larger than the view field, the inspection tool may need to scan the test structure in order to locate (i.e., localize) a defect within the test structure. When a test structure is smaller than the view field, the level of detail that is provided by the inspection tool may be reduced.

[0044] With reference to Fig. 4, an exemplary system of localizing defects on a test chip is depicted. More specifically, in one exemplary embodiment, a defect localization system 400 includes a fabrication facility 404, an in-line inspection tool 406, a parallel electrical tester 408, a processor 410, and an inspection tool 412.

[0045] In the present exemplary embodiment, a test wafer 402 with one or more test chips is fabricated in fabrication facility 404. The test wafer 402 is in-line inspected using in-line inspection tool 406. The test wafer 402 is parallel electrically tested using parallel electrical tester 408. The results of the electrical test can be analyzed using processor 410. It should be recognized that processor 410 can be a component of parallel electrical tester 408 or a separate unit. The test wafer 402 is inspected using inspection tool 412.

[0046] It should be recognized that system 400 can include additional elements or fewer elements. For example, in-line inspection tool 406 can be omitted from system 400. Alternatively and/or additionally, inspection tool 412 can be omitted from system 400.

[0047] II. Test Chip

[0048] A test chip is used to characterize integrated circuit layout and manufacturing process interactions of an actual product chip. As described above, a test chip is designed to simulate the same failure modes as an actual product chip.

[0049] More specifically, as conceptualized in Fig. 5, an actual product chip 502 can have a plurality of design pattern variations. For example, one design pattern variation can include lines of a certain line width. As depicted in Fig. 5, the design pattern variations can include a number of core design pattern variations 504. A test chip 506 can be designed to include these core design pattern variations. Test chip 506 is easier to inspect, test, and analysis than actual product chip 502. In the context of the present description, the design pattern variations on a test chip are referred to as experiments. Additionally, a test chip can also be referred to as a CHARACTERIZATION VEHICLE, which is a trademark of PDF Solutions of San Jose, California USA.

[0050] The following table lists exemplary test structures:

Name	Description	Comments
Via Chain without Neighborhood	Vertical or horizontal snaking chain of M1, M2 links connected by vias	May be wired out in "long runner" configuration
Via Chain with Neighborhood	Vertical or horizontal snaking chain of M1, M2 links connected by vias	
1-D SnakeComb BigCell	Vertical or horizontal metal lines arranged in a "grating." Edge hookups create snake between two interleaved combs	May have either parallel or perpendicular patterns in underlayer
1-D SnakeComb with SubCells	Vertical or horizontal metal lines arranged in a "grating." Edge hookups create snake between two interleaved combs. Many such SnakeComb "sub cells" arranged in an array	May have either parallel or perpendicular patterns in underlayer
Snake	Vertical or horizontal metal lines arranged in a "grating." Edge hookups create a pure snake	May have either parallel or perpendicular patterns in underlayer

Name	Description	Comments
1-D Comb	Vertical or horizontal metal lines arranged in a "grating." Edge hookups create two interleaved combs. Important area is long lines and line ends may be relaxed	May have either parallel or perpendicular patterns in underlayer
2-D Comb	Like many 1-D combs appended vertically or horizontally. Important area is line end rather than long line	Nearly identical patterns in underlayer

It should be recognized, however, that the types and numbers of test structures on a test chip may vary.

[0051] As described above, in one exemplary embodiment, the test structures of a test chip are configured for parallel electrical testing. With reference to Fig. 6, an exemplary layout 602 of a test chip is depicted. Layout 602 includes a plurality of padgroups 604 arranged in rows and columns. More specifically, Fig. 6 depicts 240 padgroups arranged in 12 rows and 20 columns. It should be noted, however, that any number of padgroups may be arranged in any number of rows and columns. Additionally, Fig. 6 depicts padgroups having a width of 1080 microns and a height of 1800 microns. It should be noted, however, that a padgroup may have any width and height.

[0052] As further depicted in Fig. 6, a padgroup 604 includes a plurality of test structures 606 and a padframe 608 with electrical probe pads 610 for the test structures 606 within padgroup 604. More specifically, padgroup 604 includes padframe 608 disposed between two columns of test structures 606 within padgroup 604.

[0053] As described above, in one exemplary embodiment, the test structures within a padgroup are electrically tested in parallel, meaning that the test structures within the padgroup are electrically tested together at approximately the same time. Thus, in padgroup 604 depicted in Fig. 6, test structures 606 within padgroup 604 are electrically tested together. Additionally, multiple padgroups 604 may be electrically tested together. For example, in one exemplary embodiment, six padgroups 604 are electrically tested together at one time.

[0054] Test structures 606 are electrically tested using a parallel tester that has a plurality of test probes that make electrical contact with probe pads 610 within padframe 608. More

specifically, for padgroup 604 in Fig. 6, 32 test probes contact the 32 probe pads in padframe 608 to electrically test the 30 test structures in padgroup 604 in parallel.

[0055] The arrangement of probe pads for test structures within a padgroup into a padframe for the padgroup facilitates parallel testing of the test structures. Additionally, locating probe pads adjacent to test structures reduces the length of the interconnection lines between the probe pads and the test structures.

[0056] By parallel testing the test structures, the size of the test structures can be decreased and/or the number of test structures on a test chip can be increased without necessarily increasing the overall time to electrically test the test chip. In turn, by decreasing the size of the test structures, a defect on the test chip can be located to a more specific location (i.e., localized) on the test chip. Additionally, in an exemplary embodiment when an inspection tool is used, the test structures can be sized to be compatible with the capabilities of the inspection tool, such as the view field and resolution of the inspection tool.

[0057] In Fig. 6, a padgroup 604 is depicted with test structures 606 that are two-terminal test structures (e.g., via chains, via combs, metal snakes, metal combs, and the like). Additionally, in Fig. 6, test structures 606 have one common terminal. In one exemplary embodiment, the common terminal can be grounded to the substrate.

[0058] Fig. 7 provides exemplary dimensions of test structures 606 and padframe 608 of padgroup 604 having 28 or 30 two-terminal test structures or devices under test (DUT's). In the present exemplary embodiment, for padframe 608, the pad size is 80 microns. The pad pitch in the vertical direction (Ypitch) is 100 microns. The pad pitch in the horizontal direction (Xpitch) is 130 microns. The width is 210 microns. The height is 1580 microns. For test structure 606, the height is 80 microns, and the width is 380 microns. The test structure types are snakes, combs, or any other two-terminal devices. The pads at the bottom of the columns are common nodes. The next row of pads may be used for neighborhood metals connections (to check for shorts to neighborhood). There are 30 DUTs per padgroup. It should be recognized, however, that these dimensions may vary.

[0059] In Fig. 8, test structures 606 in padgroup 604 of Fig. 7 are depicted as being configured as 28 via chains. Alternatively, in Fig. 9, test structures 606 in padgroup 604 of Fig. 7 are depicted as 30 comb cells.

[0060] It should be recognized, however, that test structures 606 in padgroup 604 of Fig. 7 can be configured as various two-terminal test structures. Additionally, it should be recognized that a padgroup 604 can include test structures having any number of terminals.

[0061] For example, in Fig. 10, a padgroup 604 is depicted with eight test structures 606 that are four-terminal test structures or devices under test (DUT's). It should be noted, however, that padgroup 604 can include any number of four-terminal test structures. In the present exemplary embodiment, for padframe 608, the pad size is 80 microns. The pad pitch in the vertical direction (Ypitch) is 100 microns. The pad pitch in the horizontal direction (Xpitch) is 130 microns. The width is 210 microns. The height is 1580 microns. For test structure 606, the height is 380 microns, and the width is 380 microns. The test structure types are snakecombs or any other four-terminal devices. There are eight DUTs per padgroup. It should be recognized, however, that these dimensions can vary.

[0062] In Fig. 11, test structures 606 in padgroup 604 of Fig. 10 are depicted as being configured as eight snakecomb cells. In one exemplary embodiment, each snakecomb cells depicted in Fig. 11 is configured to permit localization of a defect in a snakecomb cell to a location within the snakecomb cell.

[0063] More specifically, with reference to Fig. 12-A, assume a snakecomb cell 1202 has terminals N, C, and G. With reference to Fig. 12-B, assume now that snakecomb cell 1202 has a defect 1204. With reference to Fig. 12-C, assume that the snake comb with the defect depicted in Fig. 12-C can be characterized by electric circuit 1206.

[0064] In one exemplary embodiment, the following electrical test can be performed:

R_{gn} = force 1V at G, terminate at N, measure resistance GN
R_{gc} = force 1V at G, terminate at C, measure resistance GC
R_{nc} = force 1V at N, terminate at C, measure resistance NC

where A, B, and D are calculated as follows:

$$D = \frac{R_{gc} - (R_{gn} - R_{nc})}{2}$$

$$B = R_{gc} - D$$

$$A = R_{gn} - B$$

and:

$$\text{shortPerc (position of defect on Snake vs. Grounded side of Snake (G))} = \frac{A}{R_{gn}}.$$

[0065] Alternative, assume the following electric tests are performed:

R_{gn} = force 1V at G, terminate at N, measure resistance GN
R_{gc} = force 1V at G, terminate at C, measure resistance GC
R_{ngc} = force 1V at N, terminate at C, measure resistance NC

(R_{ngc} differs from the previous measurement method because it forces 1V at both G and N to cut off a sneak path between the G terminals of multiple snakecombs in the same padgroup.) where A,B, and D are calculated as follows:

$$X = \frac{R_{gn} - (R_{gc} - R_{ngc})}{2}$$

$$B = \sqrt{(R_{gn})^2 - R_{gn}X}$$

$$A = R_{gn} - B$$

and:

$$\text{shortPerc (position of defect on Snake vs. Grounded side of Snake (G))} = \frac{A}{R_{gn}}.$$

[0066] In one exemplary embodiment, a soft short is detected by comparing a line resistance, which can be determined based on a measured voltage, to a threshold resistance. If the line resistance is below the threshold voltage, then a soft short is detected. A hard short is also detected by comparing a line resistance to a threshold resistance. However, the threshold resistance used to detect a soft short is greater than the threshold resistance used to detect a hard short.

[0067] Additionally, in another exemplary embodiment, a soft short is detected by determining an average resistance for a number of lines that are adjacent to each other, such as those within the same padgroup. If a particular line has a resistance less than the average resistance by a specified amount, then a soft short is detected. A hard short is also detected by comparing a line resistance to the average resistance. However, the specified amount of difference between the resistance of a line with a soft short and the average resistance is less

than the difference between the resistance of a line with a hard short and the average resistance.

[0068] In Fig. 13, another padgroup 604 is depicted with eight test structures 606 that are four-terminal test structures or devices under test (DUT's). In contrast to padgroup 604 depicted in Fig. 10, padgroup 604 depicted in Fig. 13, 4 test structures 606 are formed in one layer and four test structures 606 are formed on another layer. In the present exemplary embodiment, for padframe 608, the pad size is 80 microns. The pad pitch in the vertical direction (Ypitch) is 100 microns. The pad pitch in the horizontal direction (Xpitch) is 130 microns. The width is 210 microns. The height is 1580 microns. For test structure 606, the height is 760 microns, and the width is 380 microns. The test structure types are snakecombs or any other four-terminal devices. There are eight DUTs per padgroup with 4 in each layer. Padgroup 604 has the same schematic as padgroup 604 in Fig. 10. It should be recognized, however, that these dimensions may vary. Additionally, it should be recognized that test structure can be formed on any number of metal layers, where the test structure below another test structures in another layer can be tested, and the interaction of test structures at two or levels can be measured.

[0069] In Fig. 14, a portion of an exemplary layout 602 is depicted with a plurality of padgroups 604 arranged in rows and columns. As described above, in one exemplary embodiment, six padgroups 604 can be electrically tested together at one time. In the exemplary embodiment depicted in Fig. 14, a stick 1402 labeled as "2x106 prgxx stick" in Fig. 14 includes padgroups 604 labeled as 1, 2, 3, 4, 5, and 6. In the present exemplary embodiment, padgroups 604 in stick 1402 are electrically tested together with a probe card from a parallel electrical tester.

[0070] As depicted in Fig. 14, in the present exemplary embodiment, each padgroup 604 includes eight test structures 606. Each padgroup 604 also includes four pads for each test structure 606. Thus, the padframe for each padgroup 604 includes a total of 32 pads.

[0071] As also depicted in Fig. 14, layout 602 also includes five minipadchk cells 1404 disposed between padsgroups 604 at locations labeled a, b, c, d, and e. As will be described in more detail below, each minipadchk cell 1404 includes two test structures with four pads, which are arranged as a 2x2 padframe.

[0072] Thus, stick 1402 includes a total of 212 pads ((32 pads/padgroup x 8 padgroups) + (4 pads/minipadchk cell x 5 minipadchk cells)). As depicted in Fig. 14, the 212 pads are arranged in two adjacent columns. Thus, the padframe for stick 1402, which includes the padframe from padgroups 604 and the pads from minipadchk cell 1404, is a 2x106 padframe. In the present exemplary embodiment, the padframe width is 210 microns.

[0073] In the present exemplary embodiment, stick 1402 is referenced using two parameters (prgName and prgRow). The progName parameter uniquely identifies each stick 1402 in layout 602, and the progRow parameter uniquely identifies each padgroup 604 within a stick 1402. More particularly, the parameter prgxxx is used to refer to a stick 1402. For a layout with one or two metal layers (i.e., M1/M2), two digits are used (e.g., prgxx). For a layout with three metal layers (i.e., M3), three digits are used (e.g., prog3xx). In the present exemplary embodiment, the parameter prg00 is reserved for use as a continuity pad check stick. The progName and progRow parameters can be exported as a text file. It should be recognized that the use of these parameters is exemplary and that various parameters can be used to reference stick 1402 and the components within stick 1402.

[0074] With reference to Fig. 15, in the present exemplary embodiment, stick 1402 has a floorplan height specification of 10.72 millimeters. More particularly, as depicted in Fig. 15, a height H1 includes spacing for bottom routing. A height H2 includes the overall height of the components within stick 1402. A height H3 includes spacing for labels and M3 virtual ground pads. In the present exemplary embodiment, H1, H2, and H3 are 15 microns, 10,580 microns, and 125 microns, respectively, for a total of 10,720 microns or 10.72 millimeters. It should be recognized that these dimensions are exemplary and that stick 1402 can have various floorplan height specifications.

[0075] With reference to Fig. 16, the top of height H1 is defined by the bottom edge of pads 16 and 32 of padgroup 604 labeled 1 in Fig. 14. The bottom of height H1 includes a buffer zone for butting another stick 1402 (Fig. 14). In one exemplary embodiment, the buffer zone is also required for VIA experiment routing. As described above, in one exemplary embodiment, height H1 is 15 microns.

[0076] With reference to Fig. 17, height H2 (Fig. 15) includes height H2a of padgroup 604. The top of height H2a is defined by the top edge of pads 1 and 17 of padgoup 604. The bottom of height H2a is defined by the bottom edge of pads 16 and 32 of padgroup 604.

In the present exemplary embodiment, the pad size is 80 microns x 80 microns. The pad pitch in the vertical direction (Ypitch) is 100 microns. The pad spacing in the vertical direction (Yspace) is 20 microns. Thus, height H2a is 1,580 microns ((16 pads x 80 microns/pad) +(15 spacings x 20 microns/spacing)).

[0077] With reference to Fig. 18, height H2 (Fig. 15) also includes height H2b of minipadchk 1404. As described above and depicted in Fig. 18, minipadchk 1404 includes two test structures 1802 with four pads, which are arranged as a 2x2 padframe. In the present exemplary embodiment, test structures 1802 are used to verify the operation of the probe card and the associated test system. The top of height H2b is defined by the edge of pads 16 and 32 of the padgroup above minipadchk 1404. The bottom of height H2b is defined by the edge of pads 1 and 17 of the padgroup below minipadchk 1404. In the present exemplary embodiment, the pad size is 80 microns x 80 microns. The pad pitch in the vertical direction (Ypitch) is 100 microns. The pad spacing in the vertical direction (Yspace) is 20 microns. Thus, height H2b is 220 microns ((2 pads x 80 microns/pad) + (3 spacings x 20 microns/spacing)).

[0078] With reference to Fig. 19, height H2 includes the dimensions of each padgroup (i.e., height H2a) and minipadchk (i.e., height H2b). The top of height H2 is defined by the top edge of pads 1 and 17 of the top padgroup labeled 6 in Fig. 19. The bottom edge of height H2 is defined by the bottom edge of pads 16 and 32 of the bottom padgroup labeled 1 in Fig. 19. In the present exemplary embodiment, the pad size is 80 microns x 80 microns. The pad pitch in the vertical direction (Ypitch) is 100 microns. The pad spacing in the vertical direction (Yspace) is 20 microns. Thus, height H2 is 10,580 microns ((6 padgroups x 1,580 micron/padgroup) + (5 minpadchk x 220 microns/minipadchk)).

[0079] With reference to Fig. 20, height H3 includes height H3a, height H3b, and height H3c. The top of height H3 is defined by the bottom edge of the next metal structure. The bottom of height H3 is defined by the top edge of pads 1 and 17 of the top padgroup labeled 6 in Fig. 19.

[0080] The top of height H3a is defined by the top edge of the label. The bottom of height H3a is defined by the top edge of pads 1 and 17 of the top padgroup labeled 6 in Fig. 19. In one exemplary embodiment, the label height is 18 microns. The spacing from routing

lines to the bottom of the label is 10 microns. In the present exemplary embodiment, height H3a is 28 microns.

[0081] The top of height H3b is defined by the top edge of the M3 virtual ground pad. The bottom of height H3b is defined by the top edge of the label. In one exemplary embodiment, the pad height is 80 microns. The space from the label top to the bottom of the M3 virtual ground pad is 14 microns. In the present exemplary embodiment, height H3b is 94 microns.

[0082] The top of height H3c is defined by the bottom edge of the next metal structure. The bottom of height H3c is defined by the top edge of the M3 virtual ground pad. Height H3c functions as a buffer zone. In the present exemplary embodiment, height H3c is 3 microns. Thus, height H3 is 125 microns (28 microns + 94 microns + 3 microns).

[0083] With reference to Fig. 21, in one exemplary embodiment, layout 602 (Fig. 14) includes a height H4 for stacking sticks 1402 (Fig. 14). The top of height H4 is defined by the bottom edge of pads 16 and 32 of the bottom padgroup in the upper stick in the stack. The bottom of height H4 is defined by the top edge of pads 1 and 17 of the top padgroup in the lower stick in the stack. In one exemplary embodiment, height H4 is sized to fit a minipadchk 1404 (Fig. 14), which allows for minipadchk 1404 (Fig. 14) to be included between the bottom padgroup in the top stick in the stack and the top padgroup in the lower stick in the stack. Thus, height H4 is equal to height H2a of 220 microns. Additionally, as depicted in Fig. 21, height H4a is the difference between height H4 and height H1 and H3 (i.e., H4 – H1 – H3), which is 80 microns.

[0084] With reference to Fig. 22, an exemplary layout 602 configured for deployment into a stepper square field is depicted. Layout 602 includes a stack of two sticks 1402 with height H4a between sticks 1402. Thus, in the present exemplary embodiment, the total field height of layout 602 is 21.52 millimeters (10.72 millimeters + 0.08 millimeters + 10.72 millimeters).

[0085] It should be recognized, however, that layout 602 can be configured for various dimensions. For example, layout 602 can be configured for deployment into a scanner rectangular field. A typical scanner field has a width (X) of 26 millimeters and a height (Y) of 32 millimeters. Thus, layout 602 can include a stack of three sticks 1402. In the present

exemplary embodiment, the total field height would be 32.32 mm ((10.72 millimeters/stick x 3 sticks) + (0.08 millimeters/spacing x 2 spacings)).

[0086] To better fit the height of a typical scanner field, various adjustments can be made to layout 602 to reduce overall height. For example, height H4a can be reduced from 80 microns to 10 microns. Thus, the total field height of layout 602 is reduced to 32.18 millimeters ((10.72 millimeters/stick x 3) + (0.01 millimeters/spacing x 2 spacings)).

[0087] Alternatively, with reference to Fig. 20, the M3 virtual ground pad can be redesigned into a rectangular shape having a width and height of 40 microns x 160 microns, which reduces the height H3b from 94 microns to 45 microns. Height H3 is reduced to 76 microns, which reduces the height of a stick to 10.671 millimeters. Thus, with reference again to Fig. 22, the total field height of layout 602 is reduced to 32.033 millimeters ((10.671 millimeters/stick x 3) + (0.08 millimeters/spacing x 2 spacings)). The reduced size of the M3 virtual ground pad remains large enough for an SEM inspection tool, such as the SEMVision tool produced by Applied Materials, Inc. of Santa Clara, California, USA, to focus an electron beam to inspect/view the M3 virtual ground pad for defect localization.

[0088] As another alternative, four of the five minipadchks can be removed. More particularly, with reference to Fig. 14, the minipadchks labeled a, b, d, and e are removed, and only the minpadchk in the center, which is labeled c, is retained. Thus, height H2 is reduced to 9,700 microns, which reduces the height of a stick to 9.791 millimeters. Thus, with reference again to Fig. 22, the total field height of layout 602 is reduced to 29.393 millimeters ((9.791 millimeters/stick x 3) + (0.01 millimeters/spacing x 2 spacings)). Note that a different probe card is used to test this shorter stick.

[0089] It should be noted, however, that the various dimensions provided above are exemplary, and any one or more of these dimensions may be varied. Additionally, it should be recognized that the number of pads, test structures, padgroups, sticks, and levels can be varied.

[0090] III. Parallel Electrical Tester

[0091] As described above, the test structures within a padgroup are tested together using a parallel electrical tester. With reference to Fig. 23, an exemplary parallel electrical tester

2300 is depicted. In one exemplary embodiment, tester 2300 performs automated resistance measurement and leakage current measurements.

[0092] In the present exemplary embodiment, tester 2300 is designed to enable testing of structures within die on a wafer in less than one hour, which is a speedup of 10-20 times as compared to conventional parametric testing approaches. Tester 2300 also includes the following features:

- 256 identical, independent, parallel I/O channels, each with the following capabilities: voltage and resistance measurement, source voltage or source current, and programmable pin termination;
- Resistance measurement capability from 10ohm to 100Mohm;
- Cable-out interface to prober/prober tester interface (PTI) (8 cables with 32 signals/cable);
- Standard general purpose interface bus (GPIB) interface to compatible wafer probers;
- PC-based controller with Microsoft Windows 2000 Operating System;
- Emergency Off (EMO) switches with EMO daisy-chain connections on rear panel;
- Rolling casters for ease of movement;
- Leveling feet for secure tester installation; and
- Clean room compatible design.

It should be recognized that these features are exemplary, and that any one or more of these features can be omitted from tester 2300, or any one or more additional features can be included in tester 2300.

[0093] As depicted in Figs. 23 and 24, tester 2300 includes a monitor 2302, a keyboard 2304, a measurement control (MC) unit 2306, casters 2308, and EMO 2310. MC unit 2306 includes a pin termination module 2314, a fan tray 2316, a data acquisition (DAQ) module 2318, and a tester control module 2320. DAQ module 2318 includes digital I/O pin

termination control, current/voltage sources, and voltage measurement units. It should be recognized, however, that tester 2300, MC unit 2306, and DAQ module 2318 can include fewer or additional components.

[0094] With reference to Figs. 25 and 26, an exemplary wafer tester system 2500 is depicted. In one exemplary embodiment, tester system 2500 includes parallel electrical tester 2300, wafer prober 2502, and wafer loader 2504. As depicted in Figs. 25 and 26, tester 2300 is connected to a prober tester interface (PTI) 2506 on wafer prober 2502 using cables 2508. In the present exemplary embodiment, cables 2508 are preferably 1.8 meters long and connected to the upper rear panel of MC unit 2306 (Fig. 23). As depicted in Figs. 25 and 26, tester 2300 is preferably positioned close enough to wafer prober 2502 to reduce strain on cables 2508. Ideally, as depicted in Figs. 25 and 26, tester 2300 is immediately adjacent to wafer prober 2502. Wafer loader 2504 includes one or more front opening unified pods (FOUPs) to process multiple wafers through wafer prober 2502.

[0095] With reference to Fig. 27, a system block diagram is depicted of tester system 2500. As depicted in Fig. 27, wafer prober 2502 includes an auto-loader 2704 to receive a test wafer 2702 from wafer loader 2504 (Figs. 25 and 26). Wafer prober 2502 also includes a probe card 2706 to electrically contact test wafer 2702. More particularly, in the present exemplary embodiment, probe card 2706 includes 256 pins. Thus, the 212 pads in stick 1402 (Fig. 14) can be electrically tested in parallel at one time using probe card 2706.

[0096] In the present exemplary embodiment, wafer prober 2502 is controlled by tester control module 2320 through GPIB interface 2708. More particularly, tester control module 2320 issues commands to wafer prober 2502, such as commands to position probe card 2706, lift probe card 2706 off of a stick, move to a new position, and descend to make contact with another stick.

[0097] As depicted in Fig. 27, in the present exemplary embodiment, test signals are transmitted between probe card 2706 and pin termination module 2314 through a signal bus 2716. In the present exemplary embodiment, signal bus 2716 is an 8x32 signal bus. The test signals are also transmitted between termination module 2314 and multiplexer module 2710 through signal bus 2716. The test signals are then transmitted from multiplexer module 2710 to DAQ module 2318.

[0098] As also depicted in Fig. 27, MC unit 2306 sends digital control signals to pin termination module 2314 through a digital I/O (DIGIO) 2712. MC unit 2306 also includes analog voltage sources for pin termination module 2314. Additionally, MC unit 2306 and tester control module 2320 are connected using a peripheral component interconnect (PCI) bridge 2714.

[0099] With reference to Fig. 28, a system block diagram of a portion of termination module 2314 (Fig. 27) is depicted. As depicted in Fig. 28, termination module 2314 (Fig. 27) includes a plurality of switch cards 2802, which receive test signals from probe card 2706. In the present exemplary embodiment, termination module 2317 (Fig. 27) includes 8 switch cards 2802, where each switch card can be connected to as many as 32 pins from probe card 2706. More particularly, as depicted in Fig. 28, pins 1-32 from probe card 2706 are connected to a first switch card 2802 (labeled PT1 in Fig. 28), subsequent groups of 32 pins are connected to subsequent switch cards 2802, and then pins 225-256 are connected to an eighth switch card 2802 (labeled PT8 in Fig. 28).

[00100] As also depicted in Fig. 28, each switch card 2802 is connected to DIGIO 2712 (Fig. 27) and voltage sources in MC unit 2306 (Fig. 27). More particularly, each switch card 2802 is connected to 16 DIGIO lines and 2 voltage sources.

[00101] In the present exemplary embodiment, one function of termination module 2314 (Fig. 27), and more particularly switch card 2802, is to form a resistor divider with the resisters in the device under test (DUT), selectable on-board termination resistor, and software-controlled analog voltage sources. More particularly, with reference to Fig. 29, an exemplary circuit diagram is depicted. As depicted in Fig. 29, a resistor divider is formed with the resistor R in the DUT, the termination resistor R_T, and the analog voltage source V_S. Thus, the resistance of the DUT can be determined from voltage measures V_M. Note that the DUT current (I_{DUT}) is equal to V_M/V_T, the DUT voltage is equal to $V_S - V_M$, and the DUT resistance (R_{DUT}) is equal to V_{DUT}/I_{DUT}. Additionally, in the present exemplary embodiment, resisters R_W are only used for error calculations of absolute R value.

[00102] With reference to Fig. 30, an exemplary circuit diagram of a two point resistance measurement implementation is depicted. As depicted in Fig. 30, a first voltage source (V1) is provided on channel i and a second voltage source (V2) is provided on channel j.

The DUT resistance can then be determined based on the two source voltages and the termination resistance Rt.

[00103] With reference to Fig. 31, a system block diagram of a portion of switch card 2802 (Fig. 28) is depicted. As depicted in Fig. 31, switch card 2802 (Fig. 28) includes a plurality of pin terminator circuits 3102. In the present exemplary embodiment, each switch card 2802 (Fig. 28) includes 32 pin terminator circuits 3102, where each pin terminator circuit 3102 is connected to a pin from probe card 2706.

[00104] As also depicted in Fig. 31, switch card 2802 (Fig. 28) includes a plurality of digital multiplexer (MUX) controls 3104. In the present exemplary embodiment, each switch card 2802 (Fig. 28) includes 16 digital MUX controls 3104, where each digital MUX control 3104 is connected to two pin terminator circuits 3102 and provide eight control signals to each pin terminator circuits 3102.

[00105] With reference to Fig. 32, a circuit diagram of a portion of pin terminator circuit 3102 (Fig. 31) is depicted. As depicted in Fig. 32, pin terminator circuit 3102 (Fig. 31) includes a plurality of quad switches 3202. In the present exemplary embodiment, each terminator circuit 3102 (Fig. 31) includes two quad switches 3202, where each quad switch 3202 is connected to a source voltage and four control signals. Thus, quad switches 3202 can connect the pin connected to pin terminator circuit 3102 (Fig. 31) to any of the source voltages and control signals.

[00106] With reference to Fig. 33, a system block diagram of MC unit 2306 is depicted. As described above, MC unit 2306 includes multiplexer module 2710 (Fig. 27), which receives test signals from probe card 2706 (Fig. 27). In the present exemplary embodiment, multiplexer module 2710 (Fig. 27) includes a plurality of multiplexer cards 3302 to combine the test signals received from probe card 2706 (Fig. 27). More particularly, as depicted in Fig. 28, each multiplexer card 3302 is a 32-to-1 analog multiplexer card that combines 32 channels received from probe card 2706 (Fig. 27) into one DAQ channel. In the present exemplary embodiment, eight multiplexer cards 3302 are used to combine the 256 test signals into eight DAQ channels, which are transmitted to an eight channel DAQ card 3304, which converts analog input to 16 bit digital measurements. In the present exemplary embodiment, DAQ card 3304 uses only one of the eight DAQ channels at a time.

[00107] As depicted in Fig. 33, multiplexer cards 3302 are connected to a signal conditional extensions for instrumentation (SCXI) bus 3306. DAQ card 3304 is connected to a PCI bus 3308. SCXI bus 3306 and PCI bus 3308 are connected to a local bus 3310.

[00108] As also depicted in Fig. 33, MC unit 2306 includes a digital I/O card 3312 with DIGIO 2712 to send control signals to pin termination unit 2314 (Fig. 27). More particularly, digital I/O card 3312 generates address, data, and control signals used to configure pin termination unit 2314 (Fig. 27). The address and data are decoded by termination unit 2314 (Fig. 27) to select a termination resistor, voltage source, ground, or open circuit for each probe pin on probe card 2706 (Fig. 27).

[00109] MC unit 2306 also includes PCI bridge 2714 and a voltage source 3314, which outputs 16 voltage sources to pin termination unit 2314 (Fig. 27) using a VSX 3316. PCI bridge 2714 and voltage source 3314 are both connected to PCI bus 3308.

[00110] IV. Analysis

[00111] The results of the electrical test can be analyzed to identify the location of (i.e., localize) any defects. More specifically, the location of a test structure failing the electrical test is determined based on the results of the electrical test. The results of the electrical test also can be analyzed to classify detected defects as random or systematic defects. Furthermore, the results can be analyzed to determine, model, or predict a yield.

[00112] With reference to Fig. 34, an exemplary process of defect analysis is depicted. In the present exemplary process, test chip design patterns 3402 are grouped into layout bins (e.g., bins 1-9 as depicted in Fig. 34). As depicted in Fig. 34, the test chip is fabricated and electrically tested (3404). Failure counts for each layout bin are then plotted (3406).

[00113] With reference to Fig. 35, an exemplary plot of failure rate vs. layout bins (e.g., VSTK, VNBH, VP, VBD, VLE, VBC, and VC) is depicted. The plot of failure rate vs. layout bins provides a first order indication of pattern dependency in test chip failures. With reference to Fig. 36, adding process margin splits to the plot provide a first order indication of process margin dependency in test chip failures.

[00114] With reference to Fig. 37, in one exemplary embodiment, a systematic defect identifier algorithm can analyze the test data vs. layout DOE factors (including process

margin variants) and automatically identify patterns with statistically higher fail rate. As also depicted in Fig. 37, a summary of systematic vs. random fail rates can be shown in a bar chart format with systematic failures highlighted to the user through summary bar charts.

[00115] Another approach to classifying defects as random or systematic defects and predicting yield is described in U.S. Patent No. 6,449,749, entitled SYSTEM AND METHOD FOR PRODUCT YIELD PREDICTION, issued on September 10, 2002, which is incorporated herein by reference in its entirety. It should be recognized, however, that defects can be classified and yield can be modeled using various approaches.

[00116] V. SEM Inspection Tool

[00117] As described above, the results of the analysis can be used to localize the defects using an inspection tool. When an inspection tool is used, the test chip is adapted for use with the inspection tool by sizing the test structures to be compatible with the capabilities of the inspection tool.

[00118] For example, in one exemplary embodiment, the inspection tool is a SEMVision G2 tool produced by Applied Materials, Inc. of Santa Clara, California USA. Thus, the test chip is adapted for use with the SEMVision G2 tool. More specifically, the test structures on the test chip are sized to be compatible with the view field and resolution of the SEMVision G2 tool.

[00119] Although exemplary embodiments have been described, various modifications can be made without departing from the spirit and/or scope of the present invention. Therefore, the present invention should not be construed as being limited to the specific forms shown in the drawings and described above.